

FORM PTO-1449 (SUBSTITUTE)				Attorney Docket No.: P2001,0216			
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				Appl. No.:			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Applicant: ANNALISA CAPPELLANI ET AL.			
				Filing Date: September 26, 2003			
				Group Art Unit: 2829			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
SBG	A	6,091,120	7/18/00	Yeom et al.	—	—	
SBG	B	5,089,863	2/18/92	Sato et al.	—	—	
SBG	C	5,384,479	1/24/95	Taniguchi	—	—	
	D						
	E						
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
SBG	J	42 34 528 C2	4/15/93	Germany	—	—	X
	K	42 34 777 A1	4/21/94	Germany	—	—	X
	L	2 791 177 A1	9/22/00	France	—	—	
	M	63044768	2/25/88	Japan	—	—	X
SBG	N	0 740 334 A2	10/30/96	Europe	—	—	X
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
SBG		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2 nd Edition, pp. 201-203					
SBG		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418					
EXAMINER				DATE CONSIDERED			
M.C. B.				6.7.04, 7/28/04			

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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
586	J	0 328 350 A2	8/18/89	Europe	—	—	X
586	K	02/41383 A1	5/23/02	WIPO	—	—	X
	L						
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
586		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of TiSi_2 and CoSi_2 ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269					
586		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1- μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956					
EXAMINER <i>ABD. Bz</i>				DATE CONSIDERED 6.7.04, 7/28/04			

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	L						
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>SB6</i>		Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500					
EXAMINER	<i>H.C. Bz</i>			DATE CONSIDERED			
				<i>6.7.04, 7/20/04</i>			

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